



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:

First Named Inventor: KASZYNSKI, Anne

**Art Unit: 2128**

Appln. No.: 10/627,976

**Examiner: Alhija, Saif A.**

Filed: July 28, 2003

**Confirmation No.: 4095**

For: Method for Functional Verification of an  
Integrated Circuit Model in Order to Create A  
Verification Platform, Equipment Emulator  
and Verification Platform

McLean, Virginia  
September 20, 2007

**AMENDMENT ACCOMPANYING  
REQUEST FOR CONTINUED EXAMINATION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Prior to the commencement of continued examination, please amend the  
above-identified application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins  
on page 2 of this paper.

**Remarks** begin on page 12 of this paper.